13.2 A 0.13µm CMOS EDGE/UMTS/WLAN Tri-Mode ΔΣ ADC with -92dB THD

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As data-centric applications proliferate in both cellular and local area networks, higher data-rate expectations continue to precipitate newer wireless standards, while popular incumbent standards must be retained in mobile terminals that have to shrink in size, improve power efficiency, and lower cost. Reconfigurability of wireless radios, or software defined radio (SDR), has therefore become a focus of recent research. Analog hardware is generally seen as an impediment to adaptability and its reduction a desirable outcome in the quest for SDR, especially as scaling of CMOS down to 100nm and below increasingly favors digital design over analog. High-performance ADCs are an enabling component to this end and successful GSM/WCDMA dual-mode ΔΣ modulators have been reported recently [1, 2]. This contribution describes a tri-mode ΔΣ ADC operating from 1.2V, covering 2 decades in signal frequency range and exhibiting high linearity. Its companion decimation filters are incorporated in a digital front-end to be reported separately [3].

Signal bandwidth (BW) and DR are two key parameters for ADCs intended for communications. Since the product of the two defines the achievable performance of an ADC, broader signal BW is typically accompanied by a lower DR for well established wireless standards, including the 3 most popular combined in the proposed ADC. A ΔΣ modulator naturally offers a similar trade-off between BW and resolution, making it a good starting point for a multi-standard ADC. Changing the oversampling ratio (OSR) alone, however, does not give an efficient solution because of the high BW spread between the standards. The clock frequency is therefore also set to vary according to the modes, both to avoid opamp power consumption being dictated simultaneously by the highest BW and resolution, and to enable the output to be at an integer multiple of the symbol rate of the corresponding standards. Optimization of the noise shaping characteristics of the modulator under the constraint of maximum hardware re-use resulted in sample frequencies of 26, 61.44, and 240MHz for EDGE, UMTS, and WLAN, respectively. To further optimize performance in each mode, a notch is introduced into the noise transfer function (NTF) at the edge of the signal band, programmable for each mode. To adapt power consumption to the required sampling speed, opamp input stages are biased in weak inversion, so that their BWs scale linearly with the bias current. Figure 13.2.1 shows the block diagram of the modulator, where 4th-order noise shaping is realized by a cascade of two 2nd-order modulators [4]. The modularity of the realization simplifies reconfigurability. Each modulator has a feedforward (FF) structure as well as a direct FF of the input signal to the quantizer, which avoids peaking in the signal transfer function (STF) that may amplify adjacent channel blockers. It also reduces the signal content passing through the integrators, which reduces the output swing of the latter and eases amplifier design. The quantizers have 1.5b resolution, which enhances stability and improves the SNR especially for low OSR without appreciably increasing complexity.

From the receiver planning point of view, the DR to be achieved by the ADC is set to accommodate the required SNR for signal detection in each mode, headroom for interfering blockers and margin between receiver noise and ADC noise floor. To minimize analog circuitry in the RF receiver only a 3rd-order baseband filter is assumed there. Consequently a large amount of interferers need to be processed by the ADC, which requires an exceptionally high linearity from the latter.

The schematic of the modulator is shown in Fig. 13.2.2. Sampling capacitors are shared between the signal input and the reference voltage nodes. Since the capacitors are connected to the amplifier input in every phase, offset of the amplifier is always transferred, which avoids distortion as a result of a signal-dependent offset. The summation of the FF paths is performed with an offset-compensated summing amplifier (SA). During phase φ_1, the SA performs summing, while in phase φ_2 the offset is sampled. Because active summing needs a half-period delay ($z^{-1/2}$), a fast comparator is required to reach its decision within the non-overlap period between the clock phases. Both the non-overlapping period and the comparator speed (current) are programmable to adapt to the 3 disparate sample frequencies. Bootstrapping is used for the input sampling. Out of reliability concerns, 3V thick-oxide transistors are used for part of the bootstrap circuitry. Also integrated on chip is a voltage-reference buffer that consumes <15% of the overall power.

The fact that integrators within the modulator process only quantization noise allows their output swings to be bounded within ±1/3 of the reference voltage that is programmed to 700mV for EDGE/UMTS and 350mV for WLAN. Power-efficient telescopic cascode amplifiers (Fig. 13.2.3) can thus be used even at 1.2V supply dictated by the 0.13µm CMOS technology. In order to minimize distortion due to nonlinear amplifier gain and avoid noise leakage through the modulator cascade, regulated cascoding is incorporated in the amplifier to achieve >75dB DC-gain. Linear control of the transconductance is achieved with the input stage biased in weak inversion that in turn enables linear control of the unity-gain BW (UGBW) via the bias current. In WLAN mode, the designed UGBW is close to 1GHz, where the increased bias current reduces the tolerable amplifier output swing. The reference voltage is halved in this case to reduce the signal swing accordingly.

Measured results vindicate the reconfigurability, linearity, and low-power strategies outlined above. Figure 13.2.4 shows the measured output spectra of the implemented ΔΣ modulator for EDGE, UMTS, and WLAN modes. High linearity is observed. The THD is as low as -92dB for EDGE, -89dB for UMTS, and -77dB for WLAN. The corresponding IIP3 of the 3 modes are measured separately and are found to be 34, 37, and 20dBm, respectively. In Fig. 13.2.5, the measured SNR and SNDR are plotted versus the input signal, indicating a DR of 88dB for EDGE, 79dB for UMTS, and 67dB for WLAN. Figure 13.2.6 summarizes the overall performance, where the calculated FOM lies between 0.3 to 0.9pJ/conv. For receivers with more analog filtering than the presumed 3rd-order low-pass, the reduced DR requirement would allow the ADC to operate at lower speed and power. To achieve 65dB SNDR for UMTS, the modulator requires 3.5mW. Implemented in 1P6M 0.13µm CMOS, the modulator occupies 0.4mm^2. The chip micrograph is shown in Fig. 13.2.7.

Acknowledgements:
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References:
[1] T. Burger, Q. Huang, "A 13.5mW, 185MSample/s ΔΣ-Modulator for UMTS/GSM Dual-Standard IF Reception," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1868-1878, Dec., 2001.
[2] R. van Veldhoven, "A Triple-Mode Continuous-Time ΔΣ Modulator With Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2069-2076, Dec., 2003.
[3] C. Martelli, R. Reutemann, C. Benkeser, et al., "A 50mW HSDPA Baseband Receiver ASIC with Multimode Digital Front-End," *ISSCC Dig. Tech. Papers*, pp. 260-261, Feb., 2007.
[4] O. Oliaei, P. Clement, P. Gorisse, "A 5mW ΔΣ Modulator with 84dB Dynamic Range for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 37, pp. 2-10, Jan., 2002.

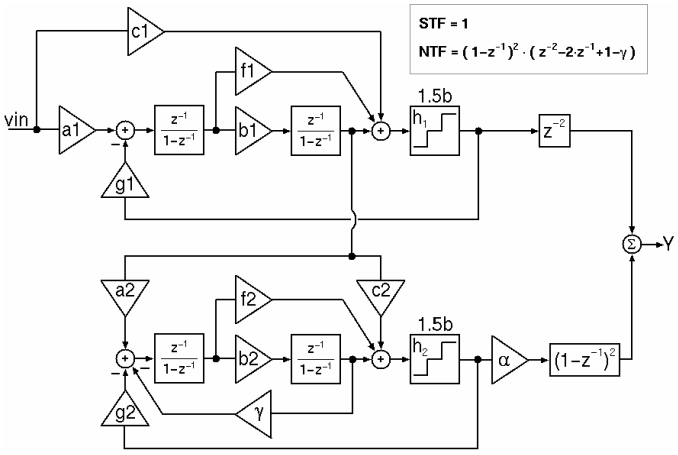

Figure 13.2.1: Block diagram of the ΔΣ modulator.

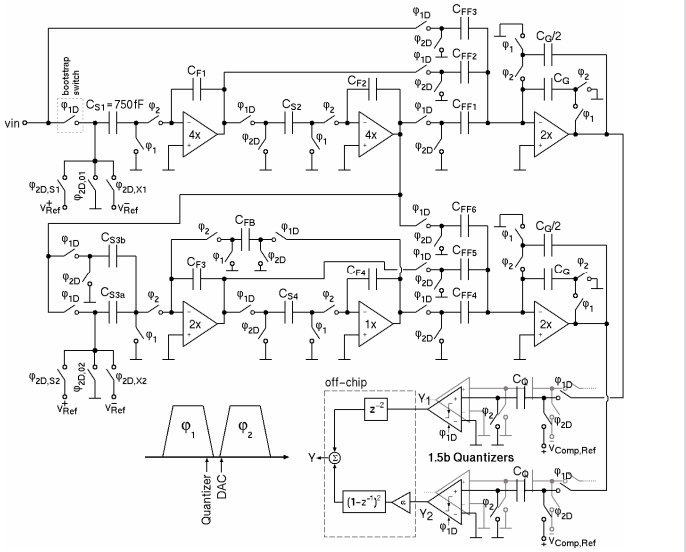

Figure 13.2.2: Schematic diagram (single-ended).

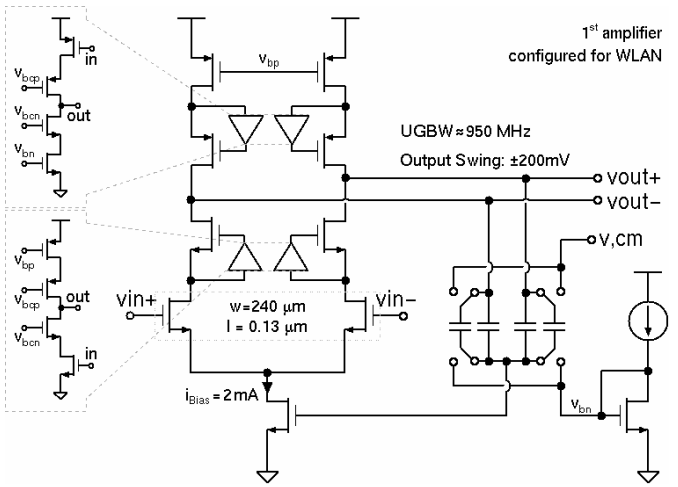

Figure 13.2.3: Amplifier schematic.

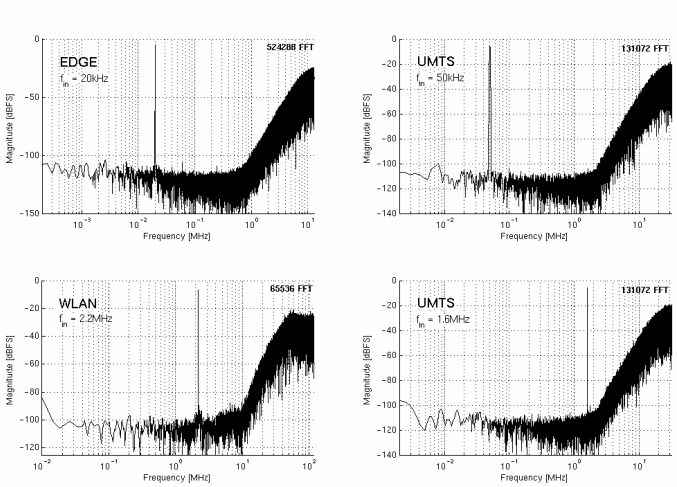

Figure 13.2.4: Measured spectra at peak SNDR.

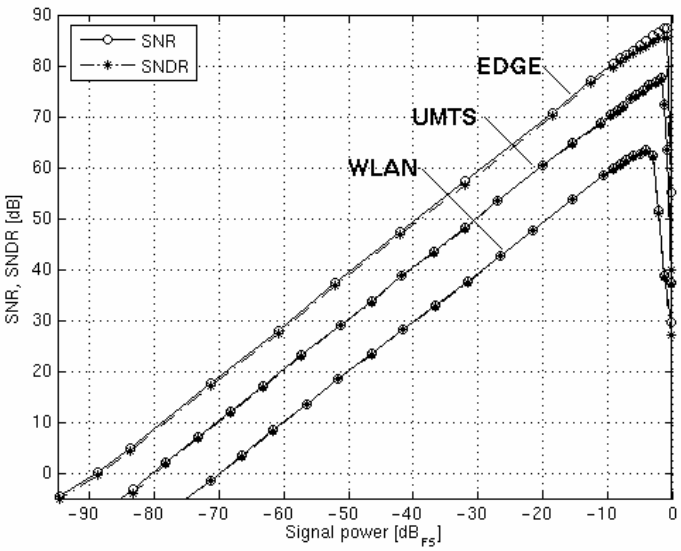

Figure 13.2.5: Measured SNR and SNDR curves.

Standard	EDGE	UMTS		WLAN
Conversion Rate	270kHz	3.84MHz		20MHz
Signal Bandwidth	100kHz	1.92MHz		10MHz
Sampling Frequency	26MHz	46.08MHz	61.44MHz	240MHz
DR	88dB	70dB	79dB	67dB
Peak SNDR	85dB	65dB	77dB	63dB
Peak THD	- 92dB	-82dB	-89dB	-77dB
iIP3	34dBm	–	37dBm	20dBm
Input Range (diff.)	$1.4V_{pp}$	$0.7V_{pp}$	$1.4V_{pp}$	$0.7V_{pp}$
FOM $\left(=\frac{Power}{2\cdot BW\cdot 2^{ENOB}}\right)$	0.9pJ/conv	0.6pJ/conv	0.3pJ/conv	0.9pJ/conv
Power Consumption	2.9mW	3.5mW	7.4mW	20.5mW
Power Supply	1.2V (3.3V for bootstrap switch only)			
Process	0.13µm 1P6M CMOS			
Core area	$0.4mm^2$			

Figure 13.2.6: Summary of measured performance.

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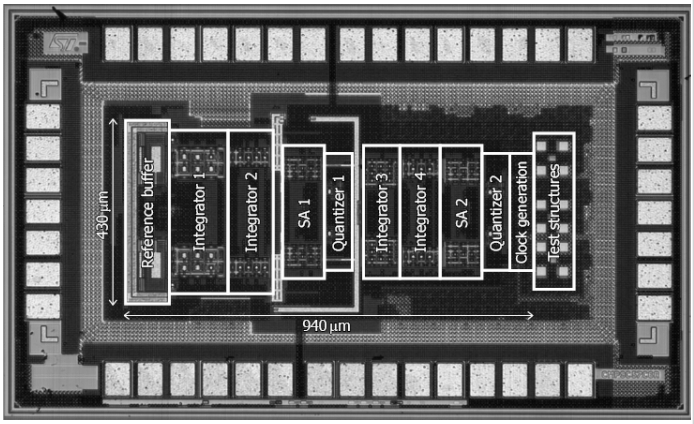

Figure 13.2.7: Chip micrograph.

